REMARKS

Reconsideration and allowance are respectfully requested in light of the above amendments and the following remarks.

Claims 13 and 14 were rejected under 35 USC §112, second paragraph, for reciting a diffusion layer of a first conductivity type that is formed so as not to be substantially present below a gate insulator film and formed to be in contact (claim 13) or separated (claim 14) from protruding portions (Office Action, section 1). The Office Action proposes that Fig. 1B illustrates a diffusion layer 7 formed under a gate insulator film 8 (Office Action section 1, second sentence). However, Fig. 1B does not illustrate the structure proposed in the Office Action. Instead, Fig. 1B illustrates that diffusion layer 7 is not substantially present below gate oxide film 8, as recited in the rejected claims. Fig. 2B illustrates this feature even more distinctly. Only protruding parts 10, p-type well 2, and p-type substrate 1 are illustrated in Fig. 1B as being substantially beneath gate insulator film 8. Diffusion layer 7 is illustrated as being adjacent to gate oxide film 8 without any portion thereof being substantially beneath gate oxide film 8.

Additionally, the Office Action proposes that it is not clear from Fig. 1B where diffusion layer 7 contacts protruding portions 10. However, Fig. 1B clearly identifies protruding

parts 10, diffusion layer 7, and the contact area where protruding parts 10 and diffusion layer 7 abut each another.

Although, Figs. 1A-1C and 2A-2C clearly illustrate the features recited in claims 13 and 14, respectively, Applicant has amended claims 13 and 14 to provide even greater clarity. For example, claim 13 has been amended to recite:

> said diffusion layer of the first conductivity type is formed so as to surround said protruding portions, and a position of an end of said diffusion layer of the first conductivity type at each of parts surrounding said protruding portions substantially coincides with a position of an end of each of said protruding portions.

Support for the subject matter added to claim 13 is provided in Figs. 1A and 1B and their accompanying descriptions in the specification. For instance, in the cross-sectional view shown Fig. 1B, both ends of gate oxide film 8 form protruding parts 10. This feature is apparent when Fig. 1B, which is a cross-sectional view of Fig. 1A along the line I-I', is associated with FIG. 1A. As may be determined by inspection, the end positions of protruding parts 10 and the end positions of diffusion layer 7, which corresponds to the recited diffusion layer of the first conductivity type, coincide with each other in the same plane.

Claim 14 has been amended to recite features similar to those added to claim 13. Support for these features is provided

in Figs. 2A-2C and their accompanying descriptions in the specification.

Claims 14 and 6 were rejected under 35 USC §102(b) as being anticipated by Pfiester (US 4,918,510). Claims 13 and 5 were rejected under 35 USC §103(a) as being unpatentable over Pfiester in view of Nagatomo et al. (US 5,164,806). Claims 11, 12, 7, and 8 were rejected under 35 USC §103(a) as being unpatentable over Pfiester and Nagatomo in view of Murakami (US 4,819,045). To the extent these rejections may be deemed applicable to amended claims 5-8, 13, and 14, Applicant respectfully traverses.

Claim 14 now recites:

> *A semiconductor device comprising:*
> *a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;*
> *a gate insulator film formed between said source side offset diffusion layer region and said drain side offset diffusion layer region;*
> *a gate electrode formed on said gate insulator film; and*
> *a diffusion layer of the first conductivity type of which an impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film, wherein:*
> *both ends of said gate insulator film in a direction substantially perpendicular to a direction from said source side offset diffusion layer region to said drain offset diffusion layer region form*

protruding portions that protrude at borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in a direction toward said diffusion layer of the first conductivity type,

said gate insulator film at said protruding portions makes direct contact with said gate electrode, and

said diffusion layer of the first conductivity type is formed so as to surround said protruding portions and so as to be separated from the protruding portions by a predetermined distance.

As recited in claim 14, a diffusion layer of a first conductivity type surrounds protruding portions, which make direct contact with a gate electrode, on both ends of a gate insulator film and is separated from the protruding portions by a predetermined distance. Together, these features reduce the leakage current and improve the withstanding voltage. Leakage current occurs in related art devices because the inversion layer formed on the semiconductor substrate surface, through the protruding portions of the gate insulator film, overlaps the diffusion layer when a voltage is applied to the gate electrode of a transistor. Figs. 2B and 2C illustrate how the claimed structure reduces or prevents the overlap of inversion layer 11 and diffusion layer 7.

The Office Action proposes that Pfiester discloses in Fig. 3 a semiconductor device in which both ends of a gate insulator film, in the channel width direction, form protruding portions 54 that protrude at the borders of source and drain side offset

diffusion layer regions 44 and 42, respectively, in the direction toward the diffusion layer of a first conductivity type 40 (Office Action page 3, lines 8-11). Continuing, the Office Action proposes that Pfiester discloses a diffusion layer 40 of a first conductivity type surrounding protruding portions 54 and separated from protruding portions 54 by a predetermined distance (Office Action page 3, lines 11-14).

However, Pfiester's Fig. 3 is clearly a cross-sectional view in the direction from source region 44 to drain region 42. In other words, Fig. 3 is a cross-sectional view in a direction parallel to line 3-3 of Fig. 1. Therefore, the proposed protruding portions 54 of gate insulator film 48 are protruding portions in a direction parallel to the direction from source region 44 to drain region 42.

By contrast to Pfiester's disclosure, the protruding portions of the gate insulator film recited in claim 14 are protruding portions in a direction substantially perpendicular to the direction from the source side offset diffusion layer region to the drain side offset diffusion layer region. The claimed structure is completely different from that of Pfiester's in this regard.

In Fig. 1A of the present application, line I-I' is the direction substantially perpendicular to the direction from

source side offset layer region 6a to drain side offset diffusion layer region 6b. Also, protruding parts 10 of gate oxide film 8 form both ends of gate oxide film 8 in this direction. On the other hand, in Pfiester's semiconductor device, the direction perpendicular to the direction from source region 44 to drain region 42 is the direction perpendicular to the line 3-3 of Fig. 1 (see line A-B of the attached drawing for reference). Pfiester discloses no cross-sectional view of the semiconductor device in the direction perpendicular to the line 3-3 of Fig. 1 and discloses neither gate insulator film end portions nor protruding portions in this direction.

Moreover, the Office Action proposes that both ends of Pfiester's gate insulator film region, in the channel width direction, are protruding portions 54 of gate insulator film 48. However, as mentioned in Applicant's Amendment, submitted April 28, 2003, the cross-sectional view of Pfiester's Fig. 3 is a cross-sectional view in the channel length direction and is not a cross-sectional view in the channel width direction. The channel width direction corresponds to the direction substantially perpendicular to the direction from the source side offset diffusion layer region to the drain side offset diffusion layer region. The channel length direction corresponds, as shown in Fig. 3 of Pfiester, to the direction from the source side offset

diffusion layer region to the drain side offset diffusion layer region. The channel width direction and the channel length direction are generally defined as shown in the indicated part of "Modern MOS Technology," which Applicant attached to the April 28, 2003, Amendment.

Applicant reemphasizes that Pfiester discloses no protruding portions of the gate insulator film in the channel width direction. Therefore, the Office Action proposal that Pfiester shows in Fig. 3 both ends of the gate insulator film region in the channel width direction form protruding portions 54 that protrude at the borders of source side offset diffusion layer region 44 and drain side offset diffusion layer region 42, in the direction toward the diffusion layer of a first conductivity type 40, is unmerited.

Furthermore, the proposed protruding portions 54 are not portions of a gate insulator film. Pfiester discloses that Figs. 3-9 illustrate the various process steps utilized in fabricating a device structure, such as that illustrated in Fig. 1 (Pfiester col. 2, lines 47-49). In the process step illustrated by Fig. 7, the exposed portions of oxide layer 54 are removed and a clean gate oxide 70 is regrown on the substrate (col. 4, lines 39-41). Clean gate oxide 70, which corresponds to reference character 48 in Fig. 3, is the gate insulator film referred to in the Office

Action. Therefore, the unexposed portions of gate oxide layer 54 remaining after the removal of the exposed portions of gate oxide layer 54 and regrowth of clean oxide layer 70 is not the gate oxide film. Thus, reference character 54 in Pfiester's Fig. 3 is not the gate insulator film and, therefore, does not constitute protruding portions of the gate insulator film. For this reason, the semiconductor device of Pfiester is completely different in structure from that recited in claim 14.

Also, claim 14 recites that the protruding portions of the gate insulator film make direct contact with a gate electrode. The Office Action proposes that Pfiester discloses in Fig. 3 a gate electrode 46 formed on a gate insulator region (Office Action page 3, lines 3-4). However, the proposed feature is not the same as the claimed feature. Pfiester's Fig. 3 clearly illustrates that gate electrode 46 does not make direct contact with the proposed protruding portions of oxide 54. Instead, the proposed protruding portions 54 of insulator film 48 are in contact with source region 52 and drain region 50 and do not make direct contact with gate electrode 46. It is well established that, to be anticipatory, a reference must disclose each and every feature of the claimed structure and must disclose the claimed structure identically.

With Pfiester's transistor, since no inversion layer is formed on the substrate surface immediately below protruding portions 54 when a voltage is applied to gate electrode 46, even if protruding portions 54 are surrounded by diffusion layer 40 of the first conductivity layer and separated by a predetermined distance, the reduction of leakage current between the inversion layer and the diffusion layer of the first conductivity type cannot be attained. Therefore, Pfiester's semiconductor device cannot provide the same benefits as does the claimed structure.

In accordance with the above discussion, Applicant submits that Pfiester does not disclose or suggest all of the features recited in claim 14. More specifically, Pfiester does not disclose or suggest the claimed features whereby: (1) both ends of a gate insulator film in a direction substantially perpendicular to a direction from a source side offset diffusion layer region to a drain offset diffusion layer region form protruding portions that protrude at borders of the source side offset diffusion layer region and of the drain side offset diffusion layer region in a direction toward the diffusion layer of a first conductivity type and (2) the gate insulator film at the protruding portions makes direct contact with a gate electrode. Therefore, allowance of claim 14 and all claims dependent therefrom is warranted.

Claim 13 now recites:

A semiconductor device comprising:
a source side offset diffusion layer region and a drain side offset diffusion layer region of a second conductivity type in a transistor formed, so as to be separated from each other, in a predetermined region in a region of a first conductivity type in a semiconductor substrate;
a gate insulator film formed between said source side offset diffusion layer region and said drain side offset diffusion layer region;
a gate electrode formed on said gate insulator film; and
a diffusion layer of the first conductivity type of which an impurity concentration is higher than that of said region of the first conductivity type and which is formed so as to surround said source side offset diffusion layer region, said drain side offset diffusion layer region and said gate insulator film, wherein:
both ends of said gate insulator film in a direction substantially perpendicular to a direction from said source side offset diffusion layer region to said drain side offset diffusion layer region form protruding portions that protrude at borders of said source side offset diffusion layer region and of said drain side offset diffusion layer region in a direction toward said diffusion layer of the first conductivity type,
said gate insulator film at said protruding portions makes direct contact with said gate electrode,
said diffusion layer of the first conductivity type is formed so as to surround said protruding portions, and
a position of an end of said diffusion layer of the first conductivity type at each of parts surrounding said protruding portions substantially coincides with a position of an end of each of said protruding portions.

The structure of claim 13 has diffusion layer end positions, of a first conductivity type, that substantially coincide with respective end positions of a gate insulator film's protruding

portions. Together, these features provide the benefits of: (1) reducing the area where the inversion layer, formed below the gate insulator film protruding portions, overlaps the diffusion layer of the first conductivity type and (2) improving the withstanding voltage. By reducing the area where the inversion layer overlaps the diffusion layer, the leakage current may be reduced.

Claim 13 recites the same features that distinguish claim 14 from Pfiester. Although claim 13 is rejected over the combination of Pfiester and Nagatomo, Nagatomo is cited in the Office Action only for teaching a diffusion layer in contact with protruding portions. Nagatomo does not cure the deficiencies of Pfeister *vis-a-vis* claim 13. Therefore, allowance of claim 13 and all claims dependent therefrom is warranted.

Moreover, the Office Action proposes that Nagatomo discloses in Fig. 4 forming a low concentration impurity region 15 between a high concentration impurity region 5a and a channel stop layer 8 (Office Action page 4, fourth paragraph). Continuing, the Office Action proposes that incorporating Nagatomo's low concentration impurity region 15 into Pfiester's structure would be obvious because the combined structure would have an increased breakdown voltage (Office Action page 4, fifth paragraph).

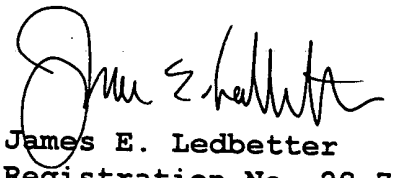
However, assuming Nagatomo's low concentration impurity region 15 were integrated with Pfiester's structure, Nagatomo teaches placing region 15 between the channel stop region, such as Pfiester's channel stop region 40 (which the Office Action analogizes to the claimed diffusion layer), and the high concentration impurity region, such as Pfiester's doped region 42. Accordingly, the end position of each of the proposed protruding portions 54 coincides with the position of a respective low concentration impurity region 15. In this case, since the gate electrode 46 does not make direct contact with the insulating film at the proposed protruding portions 54, no inversion layer is formed on the substrate immediately below the proposed protruding portions 54 when a voltage is applied to gate electrode 46. As a result, the proposed structure cannot reduce or prevent the leakage between the inversion layer and the channel stop region 40, as can the claimed structure. Therefore, allowance of claim 13 and all claims dependent therefrom is warranted for this independent reason.

In view of the above, it is submitted that this application is in condition for allowance and a notice to that effect is respectfully solicited.

If any issues remain which may best be resolved through a telephone communication, the Examiner is requested to telephone

the undersigned at the local Washington, D.C. telephone number listed below.

Respectfully submitted,



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